

Claims

What is claimed is:

1. A plasma processing system for processing a semiconductor substrate, the system comprising:
 - a processing chamber;
 - an induction coil adjacent to at least a portion of the processing chamber;
 - a first power source coupled to the induction coil to couple power to the plasma, the first power source configured to provide power to the induction coil using high power cycles and low power cycles such that greater than about 5kW of power is provided during the high power cycles;
 - a substrate support for supporting the substrate, the substrate support positioned within the processing chamber adjacent to the plasma;
 - a second power source coupled to the substrate support, the second power source configured to provide power to the substrate support using high power cycles and low power cycles such that the second power source provides high power cycles to the substrate support substantially during the time that the first power source provides low power cycles to the induction coil.
2. The processing system of claim 1, wherein the second power source is further configured such that each high power cycle provided by the second power source commences after a predetermined delay after each high power cycle provided by the first power source terminates.
3. The processing system of claim 2, wherein the predetermined delay comprises a delay sufficient to allow electrons in the plasma to cool.
4. The processing system of claim 3, wherein the predetermined delay is greater than 20 microseconds.

1 5. The processing system of claim 1, wherein the second power
2 source is further configured such that each high power cycle provided by the
3 second power source terminates after a predetermined delay after each high
4 power cycle provided by the first power source commences.

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1 6. The processing system of claim 5, wherein the predetermined
2 delay comprises a delay sufficient to facilitate coupling of power into the
3 plasma during power up cycles.

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1 7. The processing system of claim 6, wherein the predetermined
2 delay is between 1 to 6 microseconds.

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1 8. The processing system of claim 1, wherein the second power
2 source is further configured to provide high power cycles to the substrate
3 support only during a portion of time that the first power source provides low
4 power cycles to the induction coil.

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1 9. The processing system of claim 1, wherein each high power
2 cycle provided by the first power source comprises a sinusoidal signal, and the
3 low power cycles provided by the first power source comprise substantially no
4 power.

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1 10. The processing system of claim 1, wherein each high power
2 cycle provided by the first power source comprises a single pulse having a time
3 varying current, and the low cycles provided by the first power source comprise
4 substantially no power.

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1 11. The processing system of claim 10, wherein the high power
2 cycles provided by the first power source alternate between positive and
3 negative pulses.

1 12. The processing system of claim 1, wherein alternating high
2 power cycles and low power cycles provided by the second power source form
3 a square wave signal.

1 13. The processing system of claim 1, wherein each high power
2 cycle provided by the second power source comprises a sinusoidal signal, and
3 the low power cycles provided by the second power source comprise
4 substantially no power.

1 14. The processing system of claim 1, wherein the first power source
2 has a duty cycle within a range of about 5 to 30 percent.

1 15. The processing system of claim 14, wherein the second power
2 source has a duty cycle less than or equal to about one minus the duty cycle of
3 the first power source.

1 16. The processing system of claim 1, wherein the second power
2 source has a duty cycle within a range of about 25 to 75 percent.

1 17. The processing system of claim 1, wherein the first power source
2 is configured to provide an average power to the plasma within a range of about
3 200 watts to about 2 kW.

1 18. The processing system of claim 1, wherein the second power
2 source is configured to provide high power cycles comprising a DC signal
3 within the range of about negative 20 volts to negative 200 volts.

1 19. The processing system of claim 18, wherein the second power
2 source is configured to provide high power cycles comprising a DC signal of
3 about negative 50 volts.

1 20. The processing system of claim 1, further comprising a slotted
2 capacitive shield coupled between the induction coil and the plasma.

1 21. The processing system of claim 20, wherein the slotted
2 capacitive shield is coupled to ground.

1 22. A system for processing a semiconductor substrate, the system
2 comprising:

3 a processing chamber;

4 an induction coil adjacent to at least a portion of the processing
5 chamber;

6 a first power source coupled to the induction coil to couple power to the
7 plasma, the first power source configured to provide power to the induction coil
8 using high power cycles and low power cycles such that the first power source
9 has a duty cycle within a range of about 5 to 30 percent;

10 a substrate support for supporting the substrate, the substrate support
11 positioned within the processing chamber adjacent to the plasma;

12 a second power source coupled to the substrate support, the second
13 power source configured to provide power to the substrate support using high
14 power cycles and low power cycles such that the second power source provides
15 high power cycles to the substrate support substantially during the time that the
16 first power source provides low power cycles to the induction coil.

1 23. The system of claim 22, wherein the second power source is
2 further configured such that each high power cycle provided by the second
3 power source commences after a predetermined delay after each high power
4 cycle provided by the first power source terminates.

1 24. The system of claim 23, wherein the predetermined delay
2 comprises a delay sufficient to allow electrons in the plasma to cool.

1 25. The system of claim 24, wherein the predetermined delay is
2 greater than 20 microseconds.

1 26. The system of claim 22, wherein the second power source is
2 further configured such that each high power cycle provided by the second
3 power source terminates after a predetermined delay after each high power
4 cycle provided by the first power source commences.

1 27. The system of claim 26, wherein the predetermined delay
2 comprises a delay sufficient to facilitate coupling of power into the plasma
3 during power up cycles.

1 28. The system of claim 27, wherein the predetermined delay is
2 between 1 to 6 microseconds.

1 29. The system of claim 22, wherein the second power source is
2 further configured to provide high power cycles to the substrate support only
3 during a portion of time that the first power source provides low power cycles to
4 the induction coil.

1 30. The system of claim 22, wherein each high power cycle provided
2 by the first power source comprises a sinusoidal signal, and the low power
3 cycles provided by the first power source comprise substantially no power.

1 31. The system of claim 22, wherein each high power cycle provided
2 by the first power source comprises a single pulse having a time varying
3 current, and the low cycles provided by the first power source comprise
4 substantially no power.

1 32. The system of claim 31, wherein the high power cycles provided
2 by the first power source alternate between positive and negative pulses.

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1 33. The system of claim 22, wherein alternating high power cycles
2 and low power cycles provided by the second power source form a square wave
3 signal.

1 34. The system of claim 22, wherein each high power cycle provided
2 by the second power source comprises a sinusoidal signal, and the low power
3 cycles provided by the second power source comprise substantially no power.

1 35. The system of claim 22, wherein the first power source has a
2 duty cycle within a range of about 10 to 20 percent.

1 36. The system of claim 35, wherein the second power source has a
2 duty cycle less than or equal to about one minus the duty cycle of the first
3 power source.

1 37. The system of claim 22, wherein the second power source has a
2 duty cycle within a range of about 25 to 75 percent.

1 38. The system of claim 22, wherein the first power source is
2 configured to deliver high power cycles having a magnitude of greater than
3 about 5kW.

1 39. The system of claim 22, wherein the first power source is
2 configured to provide an average power to the plasma within a range of about
3 200 watts to about 2 kW.

1 40. The system of claim 22, wherein the second power source is
2 configured to provide high power cycles comprising a DC signal within the
3 range of about negative 20 volts to negative 200 volts.

1 41. The system of claim 40, wherein the second power source is
2 configured to provide high power cycles comprising a DC signal of about
3 negative 50 volts.

1 42. The system of claim 22, further comprising a slotted capacitive
2 shield coupled between the induction coil and the plasma.

1 43. The system of claim 42, wherein the slotted capacitive shield is
2 coupled to ground.

1 44. A method of plasma processing a semiconductor substrate,
2 comprising:
3 providing a processing chamber for processing the semiconductor
4 substrate using a plasma;
5 inductively coupling power to the plasma via a first power source using
6 high power cycles and low power cycles such that greater than about 5kW of
7 power is coupled to the plasma during each high power cycle;
8 coupling power to a substrate support via a second power source using
9 high power cycles and low power cycles; and
10 synchronizing the high power cycles of the second power source with
11 the low power cycles of the first power source such that the second power
12 source provides high power cycles to the substrate support substantially during
13 the time that the first power source provides low power cycles to the plasma.

1 45. The method of claim 44, wherein the step of synchronizing
2 comprises commencing each high power cycle provided by the second power
3 after a predetermined delay after each high power cycle provided by the first
4 power source terminates.

1 46. The method of claim 45, wherein the predetermined delay
2 comprises a delay sufficient to allow electrons in the plasma to cool.

1 47. The method of claim 46, wherein the predetermined delay is
2 greater than 20 microseconds.

1 48. The method of claim 44, wherein the step of synchronizing
2 comprises terminating each high power cycle provided by the second power
3 source after a predetermined delay after each high power cycle provided by the
4 first power source commences.

1 49. The method of claim 48, wherein the predetermined delay
2 comprises a delay sufficient to facilitate coupling of power into the plasma
3 during power up cycles.

1 50. The method of claim 49, wherein the predetermined delay is
2 between 1 to 6 microseconds.

1 51. The method of claim 44, wherein the step of synchronizing is
2 performed such that the second power source provides high power cycles to the
3 substrate support only during a portion of time that the first power source
4 provides low power cycles to the plasma.

1 52. The method of claim 44, wherein the step of inductively
2 coupling power to the plasma is performed such that each high power cycle
3 provided by the first power source comprises a sinusoidal signal, and the low
4 power cycles provided by the first power source comprise substantially no
5 power.

1 53. The method of claim 44, wherein the step of inductively
2 coupling power to the plasma is performed such that each high power cycle
3 provided by the first power source comprises a single pulse having a time
4 varying current, and the low cycles provided by the first power source comprise
5 substantially no power.

1 54. The method of claim 53, wherein the high power cycles provided
2 by the first power source alternate between positive and negative pulses.

1 55. The method of claim 44, wherein the step of coupling power to
2 the substrate support comprises alternating between high power cycles and low
3 power cycles to form a square wave signal.

1 56. The method of claim 44, wherein the step of coupling power to
2 the substrate support is performed such that each high power cycle provided by
3 the second power source comprises a sinusoidal signal, and the low power
4 cycles provided by the second power source comprise substantially no power.

1 57. The method of claim 56, wherein the first power source has a
2 duty cycle within a range of about 5 to 30 percent.

1 58. The method of claim 57, wherein the second power source has a
2 duty cycle less than or equal to about one minus the duty cycle of the first
3 power source.

1 59. The method of claim 44, wherein the second power source has a
2 duty cycle within a range of about 25 to 75 percent.

1 60. The method of claim 44, wherein the step of inductively
2 coupling power to the plasma is performed such that the first power source
3 provides an average power to the plasma within a range of about 200 watts to
4 about 2 kW.

1 61. The method of claim 44, wherein the step of coupling power the
2 substrate support is performed such that the second power source provides high
3 power cycles comprising a DC signal within the range of about negative 20
4 volts to negative 200 volts.

1 62. The method of claim 44, further comprising the step of disposing a
2 slotted capacitive shield between the first power source and the plasma to
3 reduce capacitive coupling.

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1 63. The method of claim 62, further comprising coupling the slotted
2 capacitive shield to ground.

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